On the Design of RF Spiral Inductors on Silicon

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Invited Paper

***Abstract*—This review of design principles for implementation of a spiral inductor in a silicon integrated circuit fabrication process summarizes prior art in this field. In addition, a fast and physics-based inductor model is exploited to put the results contributed by many different groups in various technologies and achieved over the past eight years into perspective. Inductors are compared not only by their maximum quality factors ($Q_{\max}$), but also by taking the frequency at $Q_{\max}$, the inductance value (L), the self-resonance frequency ($f_{\rm SR}$), and the coil area into account. It is further explained that the spiral coil structure on a lossy silicon substrate can operate in three different modes, depending at first order on the silicon doping concentration. Ranging from high to low substrate resistivity, inductor-mode, resonator-mode, and eddy-current regimes are defined by characteristic changes of $Q_{\max}$, L, and $f_{\rm SR}$. The advantages and disadvantages of patterned or blanket resistive ground shields between the inductor coil and substrate and the effect of a substrate contact on the inductor are also addressed in this paper. Exploring optimum inductor designs under various constraints leverages the speed of the model. Finally, in view of the continuously increasing operating frequencies in advancing to new generations of RF systems, the range of feasible inductance values for given quality factors are predicted on the basis of optimum technological features.**

***Index Terms*—Capacitance, electromagnetic induction, HF radio communication, impedance matching, inductive energy storage, inductors, integrated circuit fabrication, losses, magnetic fields, magnetic microwave devices, microwave circuits, microwave resonators, passive circuits, Q factor, resistance, resonance, thin-film inductors.**

I. Introduction

With the emergence of communication technologies, and particularly the portable and low-cost consumer applications during the past decade, the spiral inductor on silicon has established itself as a standard passive component in high-frequency silicon technologies. The extremely high frequencies, at which SiGe bipolar transistors and nowadays also CMOS devices are able to operate, have made radio-frequency (RF) circuits prone to the quality of the passive components [1]. Since the spiral inductor suffers considerably from both ohmic losses in metal and substrate losses due to the conductive silicon, this component typically exhibits the lowest quality factor (Q, defined in Section III-B) of the RF passives. Another issue with inductors on silicon, as far as current solutions go, is their excessive area consumption. Since inductors are built at the wafer surface, by using multilevel interconnect layers, they share the same complex processing as that of the active devices. Placement of the passive over the active devices to overcome this disadvantage is not a viable option in planar silicon technology. The small vertical spacing between interconnect layers and from the metal to the substrate prevent one from taking that approach [1]. This makes the spiral inductor on silicon a rather costly component. Unlike the classical radio coil, where a ferrite core was used for size reduction, ferrites cannot be applied at frequencies beyond 1 GHz due to high polarization losses and low permeability [2]. Soft ferromagnetic cores may be applicable in the future in that frequency regime, provided that eddy current losses in those electrically conductive films can be suppressed [3], [4]. This currently leaves one only with the option to build an inductor on silicon with an air core, consuming excessive chip area.

In this paper we therefore concentrate on the spiral air core inductor integrated on a silicon substrate and optimized in a tradeoff between area consumption and electrical parameters. We will not only provide a review of the research on integrated inductors in silicon technology, which has been pursued with great intensity since 1995 and is now maturing, but it is also our intention to put those results into perspective. Furthermore, we will shed light on the task of inductor optimization through process technology and layout options. This will be achieved by using a fast physics-based and predictive inductor model to explore the entire design space by simulation. This model is described in Section II, where also its validity is verified. In Section III, design and optimization guidelines are given, process techniques to improve the inductor quality are discussed, and the different modes of operation of a spiral coil structure on silicon are explained. In Sections IV and V, we adopt the optimization guidelines for a detailed discussion on the optimization of the spiral coil structure and the substrate engineering for minimum loss, respectively. Thereby, we will make extensive use of optimization routines on the basis of the model introduced in Section II. A prediction on the extendibility of integrated spiral inductor technology into future RF applications is made in Section VI, and conclusions are drawn in Section VII.

II. Circular Ring Model

With the advent of the spiral inductor in RF silicon technology, the need for fast and accurate compact inductor models becomes apparent [5]. Two generic approaches are pursued.

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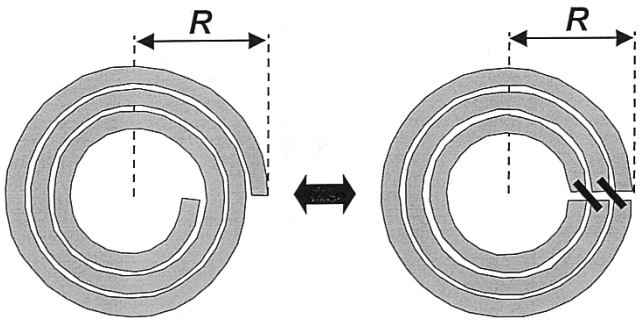


Fig. 1. Concentric-ring model of a circular spiral inductor [10].

First, the measured characteristics of a fabricated test inductor can be matched to a simple lumped-element model, as described in detail in Section III-A. Such a lumped-element model can efficiently be used in a circuit simulator, but it is nonpredictive and thus requires experimental work prior to the modeling. Alternatively to the fabrication of test devices, the inductor characteristics can be derived by using a two-dimensional (2-D) or three-dimensional (3-D) computer-aided design (CAD) tool, like Agilent's Momentum or Ansoft's HFSS. This is a practical approach but restricts one to a fixed selection of inductor designs. Further improvement would come from a model that would allow one to optimize the inductor within the circuit design process. One step in that direction came from establishing analytical relationships between each component of a lumped-element model and the technology and layout parameters from an extensive set of experiments, but this concept was not further pursued [6]. Instead, as the second generic approach to compact inductor modeling, the development of physics-based and fast inductor models has been proposed by several research groups, e.g., [7]–[10]. Most of those models have been developed for square inductors, since orthogonal or circular layouts are often not permitted in photolithographic mask generation. From a modeling point of view, however, a circular structure allows for significant reduction of the model complexity compared to a square structure. In Rejaei's model, this approach has been chosen in substituting a circular spiral coil by a set of concentric rings (Fig. 1) [10]. Since this model is fast enough if implemented in a circuit design tool, it can also be used to conduct large series of inductor calculations in an optimization task within a reasonable time frame. The error in predicting inductances and quality factors as a result of the concentric-ring approximation was found to be only about 5%. For verification of the validity of the model we fabricated and measured a set of 57 circular spiral inductors with designs for 2-, 5-, and 10-nH inductances and maximum Q's at 5, 2, and 1 GHz, respectively. A four-metal level aluminum (Al) process was used [Fig. 2(a)]. The spiral coils were built by using the M4 layer (1 μm thick), with the underpath contact at M3. The coils were therefore spaced 4 μm from the silicon substrate [as in Fig. 2(b)]. The inductors were built on a 2–5-$\Omega \cdot$ cm silicon substrate; we assumed an average resistivity of $\rho_{\rm Si} = 3.5\,\Omega \cdot$ cm in the modeling. The layout parameters were varied to meet the mentioned design goals (N $= 2$ to 8; $R = 60$ to 220 μm; $W = 4$ to 23 μm; $S = 3$ to 16 μm). The measured inductance and Q values are shown in Fig. 3(a) and(b) in comparison to the slightly higher simulated values. The error was $<$5% for the inductances and $<$10% for the Q's. The overestimation by the model resulted in part from the concentric-ring approximation, as mentioned above. Another source of error was in the uncertainty of the substrate resistivity, and finally there is an inaccuracy in S-parameter testing, which can account for an error of about $\pm$5% as well. Taking all those issues into account, we believed that we could use this model to predict general spiral inductor designs and to conduct optimization tasks with good accuracy.

This, however, still left us with the uncertainty of how relevant our findings were, since our predictions were restricted to circular spiral coils, while most published results relate to square coils. We therefore simulated the characteristics of a spiral and a square coil, having both N $= 4$, $W = 13.7$ μm, $S = 10.25$ μm, $T_{\rm M4} = 1$ μm, $T_{\rm Ox} = 4$ μm, and $\rho_{\rm Si} = 5\Omega \cdot$ cm, by using Agilent's software program Momentum. For an inductance of 3.5 nH at $Q_{\max}$ the radius of the circular spiral coil was chosen to 143 μm, and the area of the square coil was 240×240 μm^2. Fig. 4 shows that $Q_{\max}$ of the circular coil is about 12% higher. The reason for this result is in the shorter conductor length required for the circular coil to achieve a given inductance value. Consequently, the combination of dc resistance and capacitance to substrate is comparably smaller, leading to the higher $Q_{\max}$ (see Section III-A for more details). We also inserted into Fig. 4 a simulation of the circular coil structure based on Rejaei's model; it is obvious that the comparison of that model to Momentum simulations shows very good agreement. Therefore, it is reasonable to assume that the conclusions we make based on circular coil structures are qualitatively well transferable to square inductors.

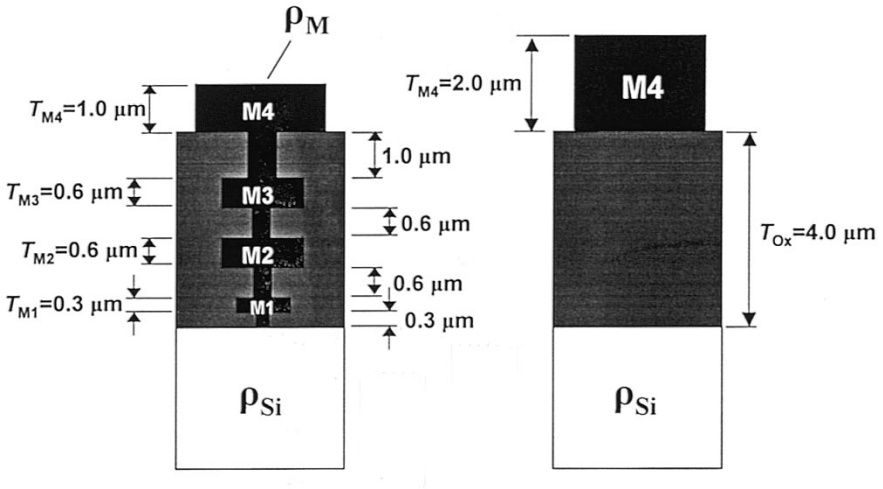
In the optimization and discussions in Section IV and V, we will particularly take advantage of the speed of the concentric-ring model. Simulations converge at an average rate of about 200 frequency points per minute. This means that it takes only a few seconds to simulate one inductor across the relevant frequency range. For the optimization tasks we could therefore use a simple random-parameter selection method. From the random data, we derived envelopes of optimum design points (see Figs. 9, 10, 12, 13, and 15).

III. Inductor Design Concepts

In this section, we discuss the inductors as an RF passive component with a predominant inductive behavior but with considerable parasitic capacitance as well. In light of this circuit-design oriented definition, we describe the electrical characteristics of the inductor (Section III-A), introduce the quality factor Q (Section III-B), discuss inductor optimization (Section III-C), and distinguish between different modes of operation (Section III-D). Herein we also focus on references to previous work on spiral inductors by others and by us.

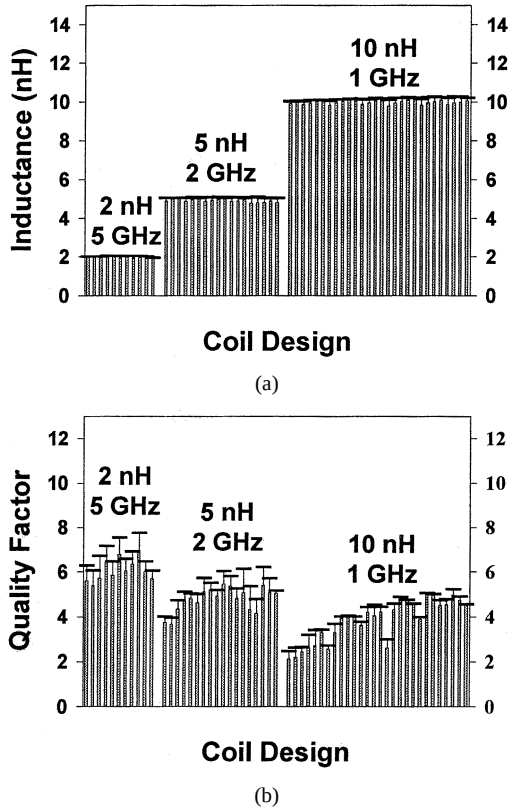
A. Inductor Integration and Lumped-Element Model

The spiral coil structure [Fig. 5(a)] has predominantly been selected for the integration of an inductor in silicon technology [11], and there are good reasons for that choice. A solenoidal coil, in comparison, has its turns alternating between two metal layers, leading to a low Q due to the relatively high via resistance



(a) (b)

Fig. 2. Cross sections of a four-level metal interconnect stack with (a) all metal layers shown and (b) only a thicker top metal layer; the thickness of the metal layers and insulating oxide layers are indicated.



(a)

(b)

Fig. 3. Comparison of measured (vertical bars) and simulated (small horizontal bars) values of (a) inductances and (b) Q-factors of 57 circular spiral aluminum coils ($T_{\rm M4} = 1\,\mu$m; $T_{\rm Ox} = 4\,\mu$m; $\rho_{\rm Si} = 2-5\,\Omega\cdot$cm $\equiv 3.5\,\Omega\cdot$cm) having optimum metal widths ($W = 4-23\,\mu$m) and spaces ($S = 3-16\,\mu$m) for given radius ($R = 60-220\,\mu$m) and numbers of turns ($\rm N = 2-8$).

[12]. Also, the area enclosed by the turns (and hence the enclosed magnetic flux) is small because of the dense spacing between the metal interconnect layers [12], [13]. The closely spaced interconnect layers also form a limitation for the third structural option, the multilevel spiral (MLS) inductor [14] [Fig. 5(b)]. The resulting large capacitance between the stacked coils considerably reduces the self-resonant frequency ($f_{\rm SR}$) in the MLS structure [14]–[17]. In spite of this shortcoming we will, however, revisit MLS inductors in Section IV-B of this paper.

Refocusing at the planar spiral coil structure in Fig. 5(a), we will now discuss the design of a spiral inductor in more detail. The lumped-element model in Fig. 6, in spite of its simplicity, can be used well to model an inductor, as mentioned in Section II. The electrical characteristics of the spiral coil itself are represented by the inductance $L_{\rm S}$, the series resistance $R_{\rm S}$, and the interwire capacitance $C_{\rm P}$. The resistance $R_{\rm S}$ is frequency-dependent due to the skin effect and the current crowding. We understand here the skin effect as an increased current density near the conductor edge due to an internal magnetic field, resulting from the RF current. Current crowding, in contrast, is defined as a change in current density resulting from the magnetic field from a neighboring conductor. Both effects are additive and cannot easily be distinguished. The skin effect can often be neglected in thin metal layers at low gigahertz frequencies or is overshadowed by parasitic capacitance effects. High-frequency leakage currents through the silicon substrate are modeled by the oxide capacitances $C_{\rm Ox}$, the resistances $R_{\rm B}$, and the silicon capacitance $C_{\rm B}$. Eddy currents in the substrate are illustrated by the loop circuit with $L_{\rm E} - M$ and $R_{\rm E}$. If the silicon resistivity is low ($< 0.1\,\Omega\cdot$ cm), eddy currents in the silicon cause a magnetic field to weaken the primary field of the metal coil. This leads to a reduced inductance $L_{\rm S}^{*} = L_{\rm S} - M$. In summary, those elements represent the electrical characteristics of an isolated inductor fairly well, but neglect that in practice the measurement RF ground (Sub) does not coincide with the true, physical RF ground ($\rm Sub^{*}$). More realistic, however, is to assume that the measurement ground (Sub) is connected through a parasitic (lumped) impedance ($R_{\rm Sub}$) to the node between $C_{\rm Ox}$ and $R_{\rm B}$ near $P_{\rm Out}$, as shown in Fig. 6. This simple model represents qualitatively the effect of a planar contact to the silicon substrate at the surface near the spiral coil of an inductor. Obviously, if $R_{\rm Sub}$ is of similar magnitude or smaller than $R_{\rm B}$, the substrate contact can have a significant effect on the inductor characteristics [18]. Also indicated in Fig. 6 is a resistance $R_{\rm Shield}$ that represents the electrical effect of a metal shield layer inserted between the spiral

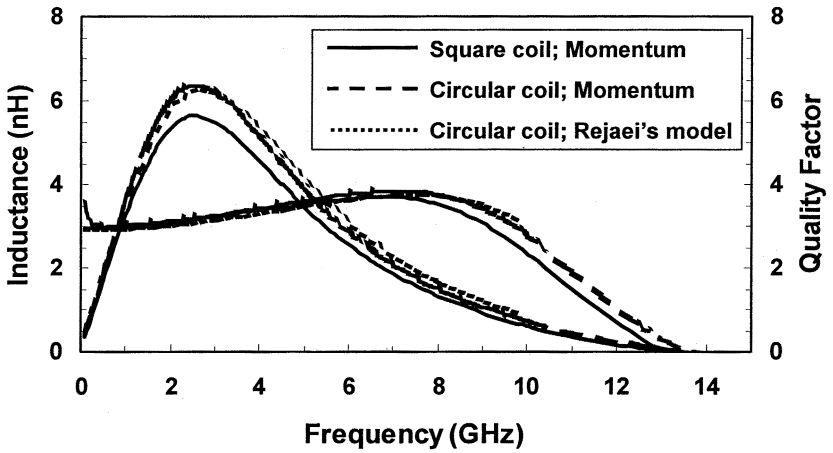


Fig. 4. Comparison of inductances and quality factors versus frequency of a square and a circular spiral aluminum inductor designed for identical inductance values near $Q_{\max}$ (Momentum simulations); also shown is a simulation of the circular coil by using Rejaei's model ($R = 120\,\mu$m; $W = 13.7\,\mu$m; $S = 10.3\,\mu$m; $\mathrm{N} = 4$; $T_{\mathrm{M4}} = 1\,\mu$m; $T_{\mathrm{Ox}} = 4\,\mu$m; $\rho_{\mathrm{Si}} = 5\,\Omega\cdot$cm).

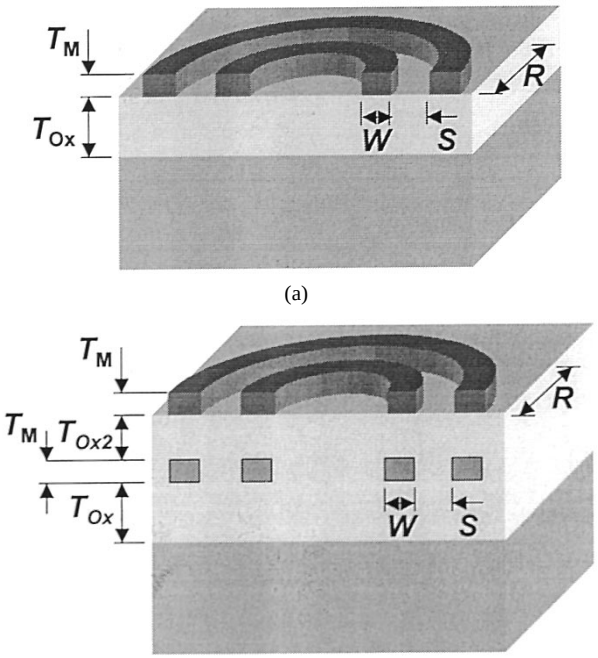


Fig. 5. Cross sections of (a) a single spiral coil and (b) two stacked spiral coils over a silicon substrate.

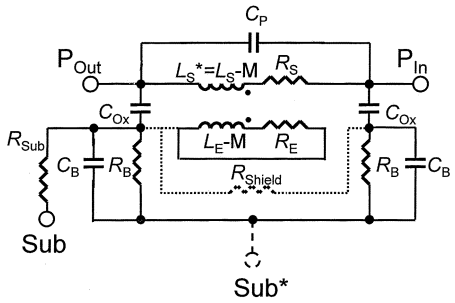
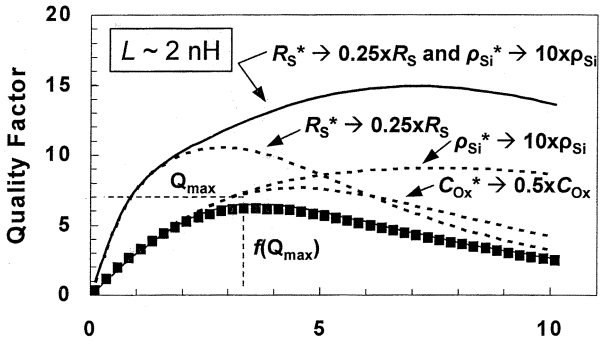


Fig. 6. Lumped-element model of a spiral inductor on a lossy silicon substrate; a planar substrate contact (Sub) and an ideal substrate contact (Sub^*) are indicated. The spiral metal coil is represented by L_{S}^*, R_{S}, and C_{P}, the leakage current through the substrate by C_{Ox}, R_{B} and C_{B}, and eddy currents in the substrate by $L_{\mathrm{E}} - M$ and R_{E} (including eddy currents in a ground shield). The resistor R_{Shield} indicates the electrical effect of a ground shield layer inserted between the spiral coil and the substrate (excluding eddy currents).

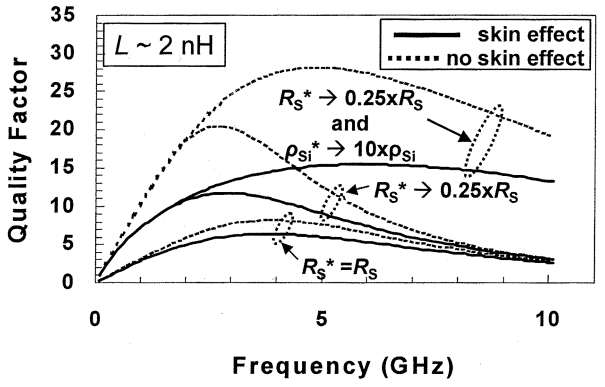
coil and the substrate (discussed in Section V-B). Such a metal shield is generally grounded, as indicated by the connection to R_{Sub}, and can cause eddy currents due to the close proximity to the spiral coil. The resistance R_{Shield} shunts the bulk resistances R_{B} and can thus have a strong effect on the inductor characteristics if $R_{\mathrm{Shield}} \ll R_{\mathrm{B}}$.

B. Quality Factor

In Fig. 7(a), the frequency dependences of the measured (data points) and modeled Q's of a sample inductor are shown. We use the conventional definition of Q, being the ratio of the stored to dissipated total energy in the component. Both the desired magnetic and the parasitic capacitive energy components are considered in this definition. This is in contrast to other definitions of Q that relate to the stored magnetic energy only [19], [20]. In RF circuit design, however, consideration of the total energy stored in the component and of the total loss is relevant. The related quality factor can simply be calculated as $Q = im(Z)/re(Z)$, with Z being the impedance of the inductor. While the inductance only shows a weak dependence on frequency (not included in Fig. 7), Q exhibits a distinct maximum $(Q_{\max})$ at a certain frequency $f(Q_{\max})$ [see markers in Fig. 7(a)]. This can easily be understood from the lumped-element model in Fig. 6. At low frequency, ωL_{S} is small and $1/\omega C_{\mathrm{P}}$ and $1/\omega C_{\mathrm{Ox}}$ are large, so that the RF signal essentially passes through the path of L_{S}, i.e., the spiral metal coil. With increasing frequency, Q grows initially as $\omega L_{\mathrm{S}}/R_{\mathrm{S}}$. At frequencies beyond $Q_{\max}$ but below resonance, ωL_{S} is larger than $(2/\omega C_{\mathrm{Ox}} + 2(R_{\mathrm{B}}//C_{\mathrm{B}}))$ but is still smaller than $1/\omega C_{\mathrm{P}}$. This situation occurs since, due to the planar spiral coil structure, $C_{\mathrm{Ox}} \gg C_{\mathrm{P}}$, C_{B}. The larger part of the RF signal now passes through the substrate, i.e., the path of C_{Ox}, causing Q to decay with frequency. Note that also the skin- and current-crowding effects lead to a limitation of $Q_{\max}$, but are in most practical design cases overshadowed by those substrate RF losses. This becomes evident from the comparisons in Fig. 7(b). With suppressed substrate losses and increased conductivity and thickness of the metal, the skin- and current-crowding effects on Q become very significant. For the typical inductor configuration [$R_{\mathrm{S}}^* = R_{\mathrm{S}}$ in Fig. 7(b)], the decay of Q beyond $Q_{\max}$ due to capacitive substrate currents domi-



(a)



(b)

Fig. 7. Simulated and measured (markers) quality factors (Q) of a circular spiral aluminum inductor ($R = 120\ \mu$m; $W = 13.7\ \mu$m; $S = 10.3\ \mu$m; $\mathrm{N} = 4$; $T_{\mathrm{M4}} = 1\ \mu$m; $T_{\mathrm{Ox}} = 4\ \mu$m; $\rho_{\mathrm{Si}} = 5 - \Omega \cdot$cm); in (a) the sensitivities to changes in metal thickness ($T_{\mathrm{M4}} \rightarrow 4\ \mu$m, i.e., $R_{\mathrm{S}}^{*} \rightarrow 0.25 \times R_{\mathrm{S}}$), oxide thickness ($T_{\mathrm{Ox}} \rightarrow 8\ \mu$m, i.e., $C_{\mathrm{Ox}}^{*} \rightarrow 0.5 \times C_{\mathrm{Ox}}$), and silicon resistivity ($\rho_{\mathrm{Si}} \rightarrow 50\Omega \cdot$cm) based on simulation are indicated; in (b) the Q with (solid) or without (dashed) consideration of the skin effect for cases of a low or normal coil resistance and a low-loss or conventional silicon resistivity are compared, indicating that capacitive substrate currents overshadow the skin effect in the conventional inductor.

nates, making the skin effect less noticeable in comparison. At a still higher frequency, self-resonance occurs within the spiral coil, i.e., through L_{S} and C_{P} (not shown in Fig. 7). The typically chosen high silicon resistivity ($\rho_{\mathrm{Si}} > 10\ \Omega \cdot$cm, i.e., large R_{B}) is responsible for self-resonance not to occur through the substrate, but through the larger C_{Ox}. If that is the case, however, the resonance frequency of the inductor is much lower than in the case sketched above [13]; we will discuss those different modes of operation in more detail in Section III-D.

C. Optimization Guidelines

If one aims at maximizing Q, then R_{S} and C_{Ox} need to be minimized and R_{B} should be as large as possible. In the case that $Q_{\max}$ should appear at a low frequency, comparably more attention should be paid to the reduction of R_{S}. The effect of a metal resistance on Q that is four time lower is illustrated in Fig. 7(a) ($R_{\mathrm{S}}^{*} = 0.25 \times R_{\mathrm{S}}$). The optimization of C_{Ox} and R_{B}, in contrast, is most important if $Q_{\max}$ should be shifted to a high-frequency value. This is illustrated in Fig. 7(a) for the cases of an oxide that is two times thicker between the metal coil and silicon ($C_{\mathrm{Ox}}^{*} = 0.5 \times C_{\mathrm{Ox}}$), as well as for a 10× higher silicon resistivity ($\rho_{\mathrm{Si}}^{*} = 10 \times \rho_{\mathrm{Si}}$). Modification of the silicon resistivity is a quite practical means for improving Q, while an increase of the oxide layer thickness is limited by mechanical stress constraints in silicon process technology. Therefore, we show in Fig. 7(a) only the combined effects of the improved resistances R_{S} and R_{B} (i.e., ρ_{Si}) as an example of a coordinated inductor optimization. These goals can be approached by an optimum design in a given process technology or by process modifications. Adhering to conventional processing, one can for instance take advantage of the available multilevel interconnects. Several metal layers can be shunted together to achieve an effectively thicker metal in the spiral coil [21]–[24]. Other ways to reduce R_{S} are to make the aluminum top metal layer thicker [25], [26] or to switch in addition to copper [27], [28] or gold [29] metallization.

Reduction of the substrate losses can be achieved by increasing the silicon resistivity, by replacing the silicon with a low-loss alternate substrate in a substrate transfer process, or by locally removing or altering the silicon through bulk-micromachining. Any of those steps should preferably be arranged as a modular addition to the core device integration process [30]. Standard silicon wafer material, grown by using the Czochralski technique, is still limited to resistivities below 100 $\Omega \cdot$cm [31], but the recently introduced magnetic Czochralski wafers may allow for resistivities up to 1 k$\Omega \cdot$cm [32]. Float-zone (FZ) silicon can routinely be fabricated with resistivities up to 10 k$\Omega \cdot$cm [25], [28], [33], though currently only up to a 6-in wafer diameter [31]. Instead of optimizing the silicon material, there are several techniques to engineer, to replace, or to remove the silicon underneath the inductor coil. For example, it is possible to transfer the role of silicon as the mechanical substrate carrier to a glued-on glass substrate, so that all silicon outside of the active device regions can be removed [34]. Local reduction of the silicon substrate losses can be achieved through an n-well formation [35], a lateral pn doping structure [36], a thick buried oxide layer [37], the formation of porous silicon [38], [39], or proton bombardment [40]. Near elimination of the substrate losses can be accomplished by local removal of the silicon [41]–[47] or by using high-aspect-ratio and surface micromachining techniques [48]–[51]. Most of those micromachining approaches have not advanced yet beyond the feasibility demonstration. Therefore, in a fairly recent approach to the utilization of micromaching in silicon RF technology, early attention is put on cost, process compatibility, and yieldability [45], [52].

D. Modes of Operation

As explained above in Section III-B, the modes of operation of a spiral coil structure on silicon can vary depending on the substrate resistivity. We had simulated $Q_{\max}$, $f(Q_{\max})$, the inductance at $Q_{\max}(L(Q_{\max}))$, and f_{SR} of the sample inductor in Fig. 7 as functions of the silicon resistivity. The results are shown in Fig. 8(a) and (b). In the simulations the impact of eddy currents in the conductive silicon was illustrated by turning this loss component on or off (solid versus dotted lines in Fig. 8). The results in Fig. 8 illustrate three distinct domains of operation, which we named "inductor mode," "resonator mode," and "eddy current mode." These operation modes have a counterpart in the TEM, slow-wave, and skin-effect modes of

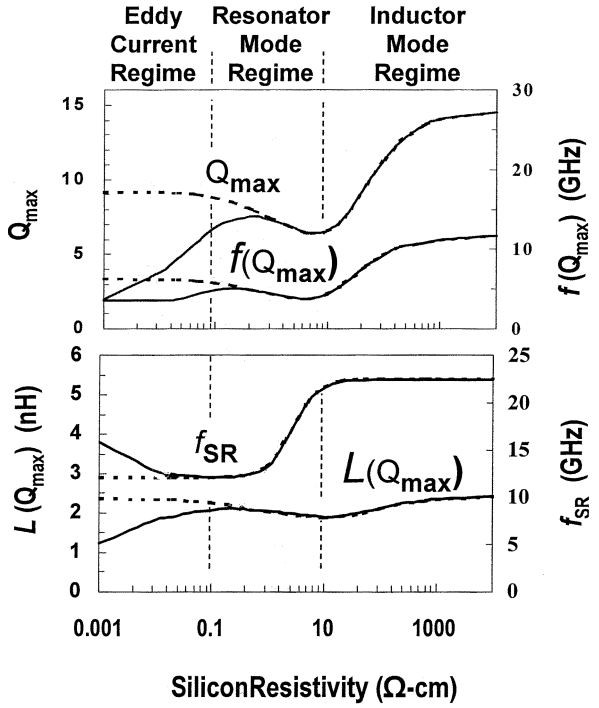


Fig. 8. Dependence of the maximum quality factor $(Q_{\max})$, the frequency at $Q_{\max}$ $(f(Q_{\max}))$, the inductance at $Q_{\max}$ $(L(Q_{\max}))$, and the self-resonance frequency $(f_{\rm SR})$ on the substrate resistivity $(\rho_{\rm Si})$ with (solid lines) and without (dotted lines) consideration of eddy currents in the substrate. The three regimes, i.e., inductor mode (resonance through $C_{\rm P}$) at $> 10\ \Omega\cdot$ cm, resonator mode (resonance through $C_{\rm Ox}$) at 0.1–10 $\Omega\cdot$ cm, and with considerable eddy current at $< 0.1\ \Omega\cdot$ cm are indicated ($T_{\rm M4} = 1\ \mu$m Al).

microstrip transmission lines on conductive substrates [53]. The analogy becomes clear if one views the N-turn spiral inductor as a system of N coupled microstrip lines. However, although one can extend the parallel-plate single-line theory of [53] to multiple lines [54], the resulting picture is not particularly simple due to various electric and magnetic couplings between the lines. The formulation, presented below, merely relies on the lumped-element representation of the spiral coil, while leaving the underlying physics of the problem intact.

At silicon resistivities beyond 10 $\Omega\cdot$ cm, one encounters the regime where the silicon substrate behaves as a dielectric represented by the capacitance $C_{\rm B}$. The substrate resistance $R_{\rm B}(\propto \rho_{\rm Si}\,\varepsilon_{\rm Si}/C_{\rm B})$ is large enough to suppress resonance through the relatively large oxide capacitance $C_{\rm Ox}$. Instead, the inductor resonates mainly through the dielectric $(C_{\rm B})$ and interwinding $(C_{\rm P})$ capacitances. Both $Q_{\max}$ and $f(Q_{\max})$ increase here with $\rho_{\rm Si}$, while $f_{\rm SR}$ is about constant and at maximum (inductor mode).

Below 10 $\Omega\cdot$ cm, the Si substrate starts to behave as a semiconductor and one observes a drastic drop of $f_{\rm SR}$, indicating that now resonance starts to occur though the substrate resistance $R_{\rm B}$ via the large oxide capacitance $C_{\rm Ox}$ (onset of resonator or slow-wave mode). Another signature of the resonator mode is the increase of $Q_{\max}$ with further reduction of $\rho_{\rm Si}$. Unlike in the inductor mode, where an increase of $\rho_{\rm Si}$ leads to higher $Q_{\max}$, due to suppression of substrate leakage currents, it is the reduction of $\rho_{\rm Si}$ that leads to an improved $Q_{\max}$ in the resonator mode. The structure consists now of a lossy inductor with $Q_{\rm L} = \omega L_{\rm S}^*/R_{\rm S}$ and a lossy capacitor $Q_{\rm C} = 1/\omega C_{\rm Ox} R_{\rm B}$, which are connected in parallel and form a resonator. Near the onset of resonator mode, i.e., at $< 10\ \Omega\cdot$cm, it is $Q_{\rm C}$ that begins to limit the resonator $Q = Q_{\rm L}Q_{\rm C}/(Q_{\rm L}+Q_{\rm C})$. Consequently, a reduction of $R_{\rm B}$ leads to an increase of Q with $\rho_{\rm Si} \ll 10\ \Omega\cdot$cm.

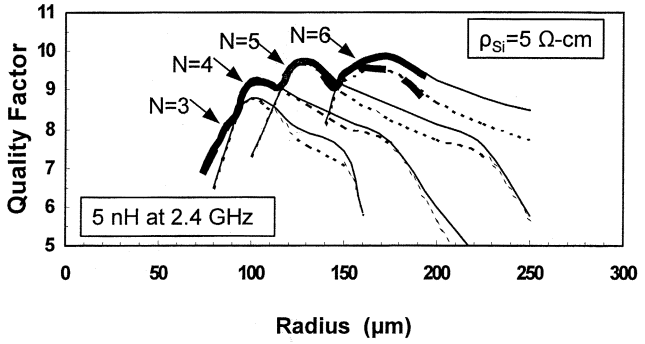
This trend is disturbed by eddy currents (skin effect) in the substrate if $\rho_{\rm Si}$ is so small that the thickness of the silicon substrate exceeds the skin depth $(2\rho_{\rm Si}/\mu_0\omega)^{1/2}$ (this occurs at $\sim 0.2\ \Omega\cdot$ cm for a $\sim$ 500–μm silicon substrate at 2 GHz). The appearance of eddy currents causes the inductance, and thus $Q_{\max}$, to decrease again, while $f_{\rm SR}$ increases due to the smaller L. Reaching resonator mode operation while suppressing eddy currents is well possible. Patterning of the conductive layer perpendicular to the eddy current vector can suppress these and thus accentuate the resonator mode. This condition can most effectively be realized by using a patterned metal layer. An insertion of a patterned metal shield between the spiral coil and the silicon substrate reaches just that goal, even though forcing resonator-mode operation was likely not the intention when introducing that structure as a means to achieve an improved $Q_{\max}$ [53]. It is important to take note that the improvement in $Q_{\max}$ with a patterned metal shield comes at the expense of a reduced $f_{\rm SR}$. A similar result could be reached with a halo substrate contact structure that provided a low-impedance shunt in the substrate for a one-port ground configuration ("Sub" and $\rm P_{in}$ at Ground in Fig. 6) [18], [56]. From the results in Fig. 8 it becomes obvious that, for operation of a spiral coil structure on silicon, the substrate resistivity should be at least 10 $\Omega\cdot$cm; for prevention from eddy currents that value should be at least 0.2 $\Omega\cdot$cm. Those numbers apply, of course, to the given geometry and substrate definition only. Slight deviations from those boundary values are expected for smaller or larger coil structures.

IV. Optimum Spiral Coil Design

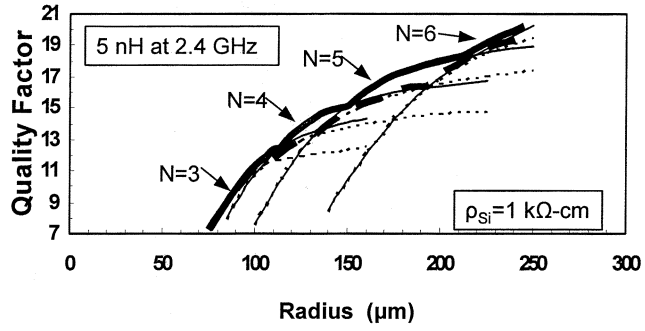
The discussions in Section III shows that optimization of a spiral inductor on a lossy silicon substrate is a quite difficult task that is further complicated by the different modes of operation. Inductor optimization involves both the layout of the metal coil structure and the substrate engineering, which cannot easily be treated separately. A distinction can be made, however, between substrate doping levels that are restricted to the inductor mode or that cover all three modes of operation. In Section IV we therefore focus on the design of the spiral inductor structure and thus on substrate doping levels of 5 $\Omega\cdot$ cm and above. We are addressing the three generic design options, i.e., the single-layer coil (Section IV-A), the shunted-metal coil (Section IV-B), and the stacked coil structures (Section IV-C).

A. Planar Coil Layout

The design of the coil of a spiral inductor is a rather complex task, even though the structure looks simple. The challenge is to choose, for a given technology with a fixed metal layer thickness, the optimum combination of N, W, S, and radius R to arrive at an optimum Q for the desired frequency. This has to be done while considering eddy current effects in the metal turns [57] and current crowding in the metal conductor [58]. Furthermore, the area occupied by the inductor should be minimum for



(a)



(b)

Fig. 9. Quality factor versus coil radius for 5-nH inductors at 2.4 GHz for given numbers of turns (N). Inductors are on (a) 5-$\Omega \cdot$ cm or (b) 1-k$\Omega \cdot$ cm silicon substrates ($T_{\mathrm{M4}} = 3$ μm (Al); Fig. 2(b)). For each inductor, the envelope of optimum design points is shown (W, $S > 3$ μm) for either constant width (dashed envelopes) or varied width W (solid envelopes).

cost reasons. This calls for a tradeoff between maximizing Q and minimizing the coil radius. To explore this, we had searched at a given N for the maximum Q's as a function of R by varying W and S. We used a metal (Al) thickness of 3 μm to highlight the substrate losses, and thus the sensitivity to R, in that case. The families of curves of identified maxima are shown in Fig. 9(a) for 5-$\Omega \cdot$ cm and in Fig. 9(b) for 1-k$\Omega \cdot$ cm silicon resistivity (thin solid and dotted curves in Fig. 9). The fat solid and dashed envelopes in Fig. 9 indicate the overall optimum designs, derived for variable conductor widths [57] and for constant conductor width, respectively. It is obvious that on the high-resistivity substrate optimum design of the 5-nH inductor at 2.4 GHz calls for larger coil area, which allows wider metal lines, thereby reducing ohmic metal losses. On the 5-$\Omega \cdot$ cm substrate, however, increasing the coil area will increase the capacitive coupling to the conductive silicon substrate, leading to higher substrate losses. The best choice in terms of $Q_{\max}$ and coil area would then be a design with $N = 5$ and 125-μm radius. Such an optimum design cannot be identified for the 1-k$\Omega \cdot$ cm substrate within the range of economically acceptable inductor sizes [Fig. 9(b)]. This nevertheless provides a 30% higher $Q_{\max}$ for the high resistivity substrate at a 125-μm radius compared to 5-$\Omega \cdot$ cm silicon or allows us to achieve the same $Q_{\max}$ at a 90-μm radius. Allowing for different track width in the coil to suppress eddy currents in metal, as mentioned above, can further optimize the designs. The increase of $Q_{\max}$ due to this design option becomes most significant for very high resistivity and large coil area, as seen from Fig. 9, [57], and [59]. The current crowding effect can be improved by changing from a conventional coil to a segmented design [60].

B. Metal Layer Shunting

Current crowding in the coil is best minimized by making the coil conductor narrow [57], [58]. Even though that reduces the current crowding, the structure will suffer from an increased coil resistance. Consequently, a thicker metal is necessary to overcome this dilemma. Shunting several metal layers in a multilevel interconnect technology together has been mentioned in Section III-C as a simple technique to provide an effectively thicker conductor without changing the process technology [21]–[24]. Shunting of metal layers, however, comes at the expense of a reduced oxide thickness between coil and substrate (T_{Ox} in Fig. 5). The C_{Ox} therefore becomes larger and Q decays at a lower frequency compared to a single-layer coil built by using only the top metal. Metal shunting therefore allows one to optimize an inductor in a conventional integration process by maximizing Q and by shifting $Q_{\max}$ to the desired frequency $f(Q_{\max})$ [24]. The tradeoff between reducing R_{S} and minimizing C_{Ox} had been addressed experimentally in our earlier work [24]. There it was assumed that large coil areas are required to accommodate the high number of turns for achieving large inductance values. One outcome of this concept was that $Q_{\max}$ of the large coils occurred at lower frequencies compared to small coils. Shunting provided a benefit for high numbers of turns, while for small inductors it was advantageous to build the coil at the top metal level only [24]. For the study presented in this paper, here we evaluated metal shunting for the cases of the fixed frequencies 900 MHz, 1.8 GHz, and 2.4 GHz. Optimum coil layouts for various inductance values were found from a large series of calculations with parameter variations, of which the envelopes of maximum Q's are plotted in Fig. 10 (see also Section II). The cases of a single M4 layer, shunted M3/M4 layers, and shunted M2/M3/M4 layers were compared (metal $=$ Al). For each of these cases there was an optimum inductance value, at which the highest Q was achieved. Below that inductance the ohmic losses in the spiral coil dominated, while above that inductance substrate losses were most significant (see Fig. 10). That optimum point was shifted to a lower inductance value for the M2/M3/M4 coil compared to the M3/M4 and the M4 inductors. Consequently, if one considers a fixed frequency, the decision for a certain shunting scheme is different from the one pointed out in [24]. Layer shunting is less advantageous at high inductance values, where substrate losses dominate. This trend is stronger at high frequency [Fig. 10(c) versus Fig. 10(b) versus Fig. 10(a)]. It is further obvious from Fig. 10 that the overall maximum quality factor is achieved at 1.8 GHz [Fig. 10(b)]. At 900 MHz, Q was limited by the area constraint [Fig. 10(a)], while at 2.5 GHz the maximum Q was set by the substrate losses [Fig. 10(c)]. It is evident that with higher substrate resistivities the regime, in which coil losses dominate, will shift to higher inductance values.

C. Stacked Spiral Coils

In spite of the current crowding and eddy current phenomena in the metal coil described in Section IV-A, mutual coupling

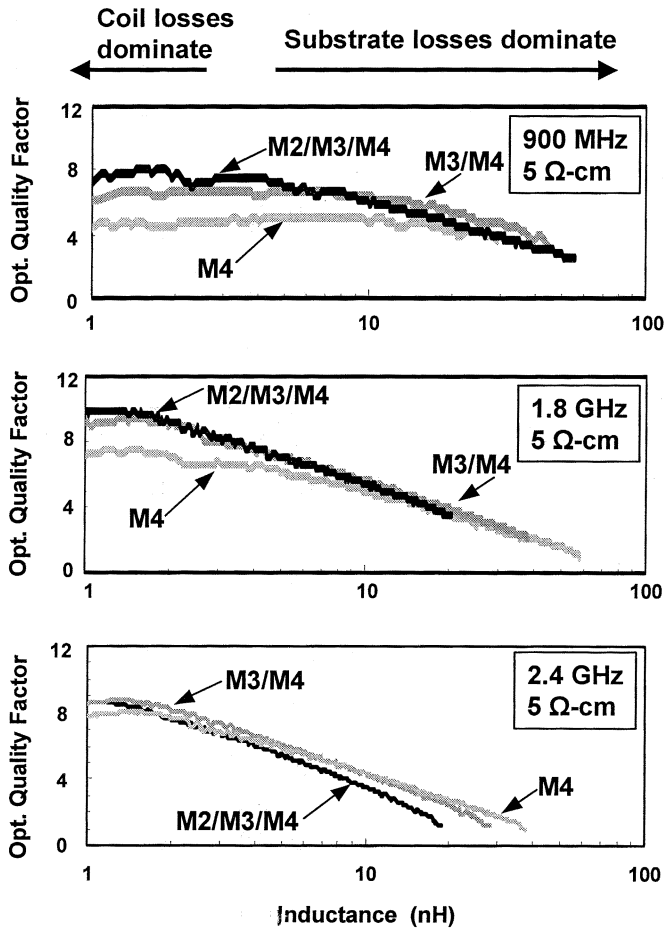


Fig. 10. Envelopes of maximum quality factors at (a) 900 MHz, (b) 1.8 GHz, and (c) 2.4 GHz versus inductances for optimized inductors in a four-level metal process ($T_{\mathrm{M4}} = 1\ \mu$m (Al); Fig. 5(a)) on a 5-$\Omega \cdot$ cm substrate, derived from simulations with random variations of W, S, N, and R ($R < 200\ \mu$m; W, $S > 3\ \mu$m; $T_{\mathrm{M4}} = 1\ \mu$m). Shunting of three (M2/M3/M4) or two (M3/M4) metal layers is compared to inductors built at the top metal layer (M4).

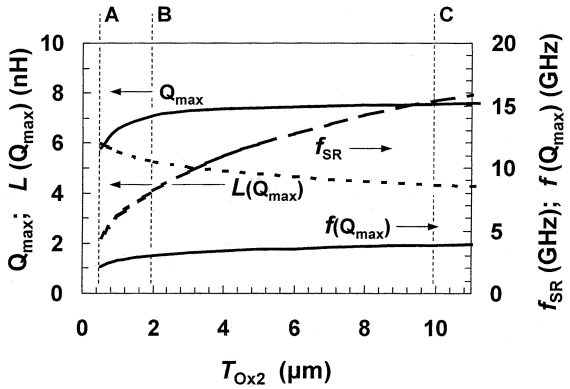


Fig. 11. Effect of coil spacing (T_{Ox2}) on maximum quality factor ($Q_{\max}$), frequency at $Q_{\max}$ ($f(Q_{\max})$), inductance at $Q_{\max}$ ($f(Q_{\max})$), and resonance frequency (f_{SR}) for an inductor consisting of two identical stacked 2-nH coils on a 5-$\Omega \cdot$ cm substrate ($N = 4$, $R = 120\ \mu$m, $W = 13.7\ \mu$m, $S = 10.3\ \mu$m). Designs for typical vertical interconnect spacing ("A"), an optimum combination of inductance per area and $Q_{\max}$ ("B"), and widely spaced coils ("C") are indicated.

between the turns in a spiral coil is essential to achieve a high inductance per area. In a planar coil structure, such coupling occurs only laterally. Since a separate metal layer is required anyhow to provide an underpath from the inner end of the coil to the outside, this metal layer may as well be used to build a second spiral coil that overlaps with the first coil [Fig. 5(b)]. Such a stacked spiral coil structure provides an increased inductance per area (for an identical sense of turn in coils) compared to two individual coils, but has a reduced f_{SR} due to the high capacitance between the coils if the spacing is small [14]. Referring to the lumped-element model in Fig. 6, this additional capacitance component is part of C_{P} and thus has a direct impact on f_{SR}. The spacing between the stacked coils is restricted by the maximum thickness of the oxide layer that can be deposited onto the wafer. The effect of the coil spacing on inductance, $Q_{\max}$, $f(Q_{\max})$, and f_{SR} becomes obvious from the simulation results in Fig. 11, which have been achieved for a fixed layout of the two 2-nH Al-coils ($N = 4$; $R = 120\ \mu$m; $W = 13.7\ \mu$m; $S = 10.3\ \mu$m). Three distinct design points are indicated in Fig. 11. For the small coil spacing between subsequent metal layers in a multilevel interconnect scheme, the inductance is increased by $\sim$50% due to the additional vertical mutual coupling (Design "A"). This comes, however, at the expense of a $\sim$20% reduction in $Q_{\max}$, a shift of $Q_{\max}$ to a somewhat lower frequency, and a drastically reduced f_{SR} compared to effectively de-coupled stacked coils (Design "C"). If one aims for an optimum combination of inductance per area and $Q_{\max}$, one would choose design "B" at 2-μm coil spacing (maximum of the product $L \times Q_{\max}$). This design still suffers from a considerable reduction of f_{SR}. A high f_{SR} is only achieved in design "C," though one loses the advantage of the increased inductance per area due to the weak vertical mutual coupling. The stacked-coil inductor therefore operates at small coil spacing in the resonator mode, but differently from the observations in Section III-D both the decay of Q beyond $Q_{\max}$ and the f_{SR} are affected here by the interwire capacitance C_{P}. The increase in inductance per area can be 1.5$\times$ compared to two widely spaced stacked coils and 3$\times$ compared to the single 2-nH coil. Even higher inductance-per-area values are feasible, but then the structure clearly operates as a LC resonator (see converging f_{SR}- and $f(Q_{\max})$-curves in Fig. 11 at minimum T_{Ox2}). True inductor operation is only achieved at large coil spacing, but with a twofold increase in inductance per area compared to a single spiral coil.

V. Minimization of Substrate Losses

Differently from the discussions in Section IV we will now treat all modes of operation of the spiral coil structure. We will focus on two distinct types of substrates, i.e., the uniformly doped silicon substrate (Section V-A) and the case of a metal ground shield between the spiral coil and the silicon substrate (Section V-B). Coil metal thicknesses of 2 μm and 3 μm, respectively, have been chosen to suppress ohmic losses in the coils and thus highlight the substrate losses to be studied.

A. Silicon Substrate Losses

It had been discussed in Section III-C that $Q_{\max}$ results from an optimum tailoring of the ohmic losses in the spiral coil and the substrate losses. The maximum Q at each inductance value,

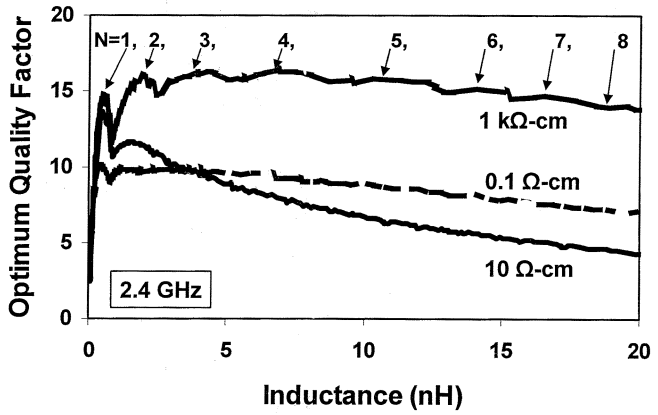


Fig. 12. Envelopes of maximum quality factors versus inductances at 2.4 GHz for 0.1-, 10-, and 1-k$\Omega \cdot$ cm substrate resistivities, derived from simulations with random variations of W, S, N, and R ($R < 200\ \mu$m; W, $S > 3\ \mu$m; $N = 1-8$) and with the structure depicted in Fig. 2(b) ($T_{\mathrm{M4}} = 2\ \mu$m; (Al)).

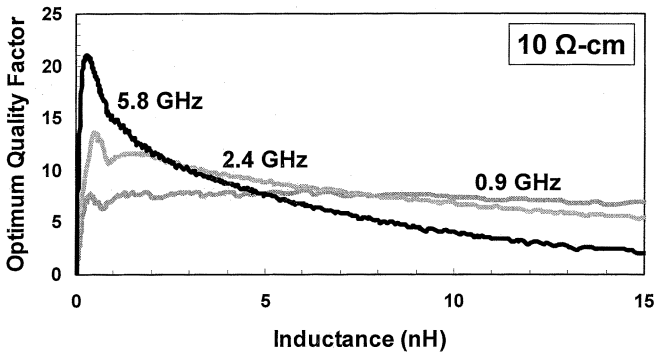


Fig. 13. Envelopes of maximum quality factors versus inductances at 0.9, 2.4, and 5.8 GHz for a 10-$\Omega \cdot$ cm substrate, derived from simulations with random variations of W, S, N, and R ($R < 200\ \mu$m; W, $S > 3\ \mu$m; $N = 1-8$) and with the structure depicted in Fig. 2(b) ($T_{\mathrm{M4}} = 2\ \mu$m).

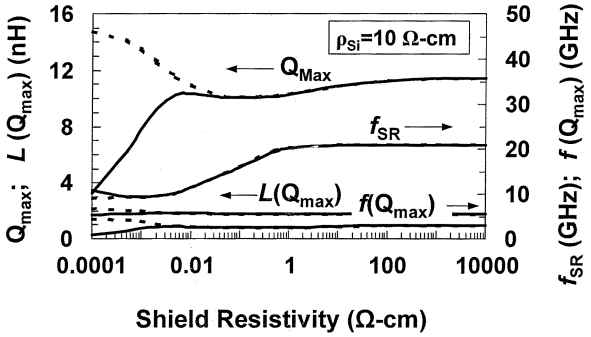


Fig. 14. Electrical characteristics of a 2-nH inductor with a spiral coil (3 μm Al) separated from a 10-$\Omega \cdot$ cm silicon substrate by a 1-μm-thick grounded shield (spacing: coil/shield $= 2\ \mu$m; shield/Si $= 1\ \mu$m; $N = 4$, $R = 120\ \mu$m, $W = 13.7\ \mu$m, $S = 10.3\ \mu$m). The maximum quality factor ($Q_{\max}$), the frequency and inductance at $Q_{\max}$ ($f(Q_{\max})$; $L(Q_{\max})$), and the self-resonance frequency (f_{SR}) are drawn versus the shield resistivity for cases with (solid lines) and without (dotted lines) eddy current effects.

while aiming at a certain frequency, is a result of an optimum design based on coil radius, number of turns, and conductor width and space. We had searched 20 000 different designs to find the $Q_{\max}$'s for inductance values up to 20 nH at 2.4 GHz and for silicon resistivities of 0.1, 10, and 1 k$\Omega \cdot$ cm. In the random search, N was allowed to range from 1 to 8 and the coil radius was constrained to 200 μm. The results from this search task are shown in Fig. 12. At 1-k$\Omega \cdot$cm substrate resistivity, one can clearly identify the (full) numbers of selected turns from the contour of the envelope. A $Q_{\max}$ of about 15 could be achieved throughout the considered inductance values above 1.5 nH. This shows that, due to the high silicon resistivity, the decay of Q beyond $f(Q_{\max})$ is closely related to C_{P} rather than C_{Ox} (larger R_{B} in the model of Fig. 6). This means that then parameters related to the lateral coil design will at first order affect $Q_{\max}$. Those parameters change roughly in proportion as one varies the design and thus the inductance value, leading to the fairly constant optimum Q versus L in Fig. 12 at 1-k$\Omega \cdot$ cm substrate resistivity. In contrast, for the 10-$\Omega \cdot$cm substrate, relatively lower $Q_{\max}$ values were determined for large inductances, indicating the effect of the capacitive loss currents through C_{Ox} and R_{B}. The larger the impedance of the L_{S}-path in the model of Fig. 6, consequently the stronger is the effect of leakage through the C_{Ox}-path. As the silicon resistivity is reduced to 0.1 $\Omega \cdot$ cm, however, the dependence of $Q_{\max}$ on L is smaller again. At this low substrate resistivity, the coil structure operates in the resonator mode, yet before eddy currents in the substrate become strongly apparent (see Fig. 8). (This predicted effect has experimentally been verified by us, but we do not present that data here.) The case of the 10-$\Omega \cdot$ cm substrate stands for the typical inductor operating in inductor mode and having considerable losses in both the metal coil and the silicon substrate. As stated earlier in Section II and identified in Section IV-A, ohmic losses in the coil weigh comparably more at low frequencies, while losses due to leakage currents through the silicon dominate at high frequencies. The design optimum moves therefore at low frequency against the maximum area limit [see, e.g., Fig. 10(a)]. Consequently, the dependence of the feasible $Q_{\max}$ on the inductance value is more pronounced at a high target frequency, as shown in Fig. 13. Therefore, the higher the target frequency is, the narrower becomes the range of feasible inductances for a given $Q_{\max}$. This aspect will further be addressed in Section VI.

B. Substrate Shields

In Section III-D, we had indicated that the effect of the substrate losses can strongly be influenced by a patterned or solid conductive ground shield layer placed between the spiral coil and the substrate. This can be a metal layer or a higher resistive polysilicon film offered by the integration process [55]. The dependencies of $Q_{\max}$, $f(Q_{\max})$, $L(Q_{\max})$, and f_{SR} on the resistivity of a 1-μm-thick shield layer are illustrated in Fig. 14 for a 10-$\Omega \cdot$ cm silicon substrate and a 3-μm-thick Al layer to form the coil. In that figure, the cases with and without eddy currents in the shield and the substrate are compared. The qualitative dependencies of the above-mentioned parameters on the shield resistivity are at first view similar to those shown in Fig. 8, where the metal shield was not present and the substrate resistivity was varied. There are, however, considerable differences. The decay of f_{SR} from high to low resistivities in Fig. 14 is not as sharp as that in Fig. 8; this results from the additional leakage currents flowing through the 10-$\Omega \cdot$cm silicon substrate. The effect of eddy currents illustrated in Fig. 8 and Fig. 14 are similar, however, because the additional eddy currents in 10-$\Omega \cdot$ cm silicon are insignificant (see Fig. 8). Focusing at $Q_{\max}$ in Fig. 14,

one notices that the highest $Q_{\max}$ can be achieved at low shield layer resistivity, provided that eddy currents can be suppressed. It has been shown that, by patterning the shield layer perpendicular to the currents in the spiral coil, this is indeed possible [55]. Such a patterned ground shield was advertised as a structure that protects from substrate losses, leading to a higher $Q_{\max}$ than without that shield [55]. Our simulation results confirm that a 30% higher $Q_{\max}$ is possible with the use of a ground shield, but that advantage comes at the expense of a strongly reduced $f_{\rm SR}$; the structure thus operates in resonator mode. A similar behavior was observed for an inductor coil combined with a halo substrate contact [18], [56]. Both the patterned shield layer and the halo substrate contact form a low-resistive shunt of the silicon ($R_{\rm Shield}$ in Fig. 6), but they cannot prevent eddy currents in a highly conductive silicon substrate from affecting the inductor characteristics. This could only be achieved by terminating the magnetic field at the shield, which would in fact *require* that eddy currents be flowing in the shield layer [61]. The only possibility to form an effective shield, terminating both magnetic and electric fields, would be to use a low-resistive blanket metal layer that is spaced sufficiently from the spiral coil. The required spacing would need to be as large as 150 μm [62]. A patterned metal ground shield is, however, effective in terminating an electric field to prevent RF crosstalk through the substrate [63]–[65]. Blanket polysilicon shields have been proposed in place of patterned metal for the same purpose [55]. Poly shields have resistivities in the range of 0.001–0.01 $\Omega \cdot$ cm, which is just at the edge of the steep eddy current onset (Fig. 14).

VI. Technology Scaling

The final question to address in this paper is certainly up to which frequencies spiral inductors can be used in monolithic RF circuit design. We have therefore determined the range of inductances on basis of the Q's required for frequencies up to 20 GHz (Fig. 15). Our simulator was used to maximize Q at the individual frequencies by varying W, S, N, and R. Copper was considered here in place of aluminum, and a metal thickness up to 4 μm was permitted. The substrate resistivity was limited to 1 k$\Omega \cdot$cm, and *radii* not higher than 200 μm were allowed. Those constraints are in line with economic aspects and the best possible processing features available today for practical inductor integration [25], [28]. The results are shown in Fig. 15. The maximum inductance values, for example, $Q = 10$, decrease above $\sim$3 GHz with frequency due to substrate losses. Below $\sim$3 GHz, the ranges of inductance become smaller with frequency reduction because of metal losses in the coil and the area constraint. It can be seen from the grey ωL-contours in Fig. 15 that a specific impedance can be maintained in technology scaling for the given Q's of 10 and 20 at $>$3 GHz, while for $Q = 30$ the constraint in silicon resistivity becomes well noticeable and limits the impedance values. The adjustment of the inductor quality with technology scaling becomes more difficult, however, if one assumes that Q be increased proportionally with frequency (see dashed grey lines for $Q =$ const. in Fig. 15). Then, e.g., at 10 GHz a maximum impedance of 300 Ω can be realized with $Q \sim$23, while at 5.8 GHz only $Q \sim$13.5 is required, therefore extending the impedance range to $\sim$ 1 kΩ. The considerations based on the conditions $Q =$const. and $Q \propto$ freq. only provide

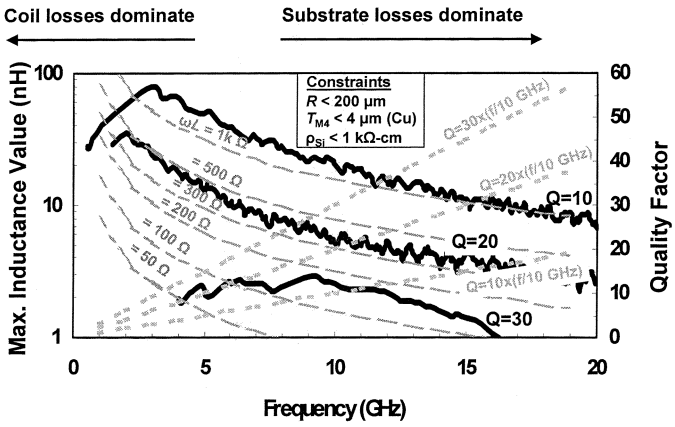


Fig. 15. Envelopes of maximum inductances for given quality factors between 10 and 30 for limited metal thickness ($T_{\rm M4} < 4$ μm Cu), silicon resistivity ($\rho_{\rm Si} < 1$ k$\Omega \cdot$ cm), and radius ($R < 200$ μm). The dominances of the constraints in metal thickness at low frequencies and in silicon resistivity at high frequencies are quite noticeable.

a general insight into the upper limitations in inductor design with technology scaling. It will depend on the cleverness in RF circuit design how far up in frequency spiral inductors can realistically be used. While there is in principle no lower limitation in inductance values, there is certainly a practical limit. As the interconnect self-inductances become comparable to the inductance value of the discrete inductor, it becomes very difficult to design and layout an RF circuit. That limit is typically near 0.5 nH. It can therefore be presumed that inductors can practically well be applied up to 10 GHz. At frequencies $\gg$10 GHz, discrete passive components will have to be substituted by distributed passives, requiring the integration of transmission lines on a silicon chip. Because of very large dimensions of transmission lines at $<$30 GHz, an interesting challenge presents itself for frequencies of 10–30 GHz, entertaining the application of periodic transmission lines, patterned ground planes, or integration of ferromagnetic and high-ε materials on silicon.

VII. Conclusion

The optimization of a spiral inductor on silicon is, in spite of the simplicity of the structure, a complicated task. More insight can be gained by making a clear distinction between the three modes of operation of a spiral inductor over a lossy substrate. The boundaries are set by the substrate doping: a spiral coil operates in inductor mode at a silicon resistivity above $\sim 10\,\Omega\cdot$cm, resonator mode occurs in the range of $\sim$ 0.2–10 $\Omega \cdot$ cm, and below $\sim 0.2\,\Omega \cdot$cm the structure works in the undesirable eddy current regime. If one expects from a spiral coil structure to feature a maximum Q at a much lower frequency than its resonance point, design for operation in inductor mode is required. Resonator mode operation can be of interest for coil implementation in an LC tank circuit, since an increase in Q by roughly 50% is possible at the given frequency. Both ohmic losses in the spiral coil and substrate losses have to be tailored to optimize an inductor for maximum Q at the target frequency. In a given process technology, there is a tradeoff between the maximum Q and the coil area, which one has to take into account. With today's economically reasonable process feature improvements,

the widest range of inductance values for a given Q can be provided near 2.4 GHz. RF circuit design based on discrete inductor components can safely be expected up to 10 GHz, while far beyond that range a transition to distributed passive components may be required.

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